REMARKS

Claims 5-13 are pending in this application. By this Amendment, the specification and claims 5, 9 and 10 are amended. Claim 5 is amended to recite features supported in the specification at, for example, paragraphs **[0043]**, **[0046]**, **[0048]** – **[0050]** and Figs. 8(f), 9(b) and 10(c). Claim 9 is amended to correct antecedence having no effect on patentability. Claim 10 is amended to correct claim dependency. No new matter is added by any of these amendments.

Reconsideration based on the following remarks is respectfully requested.

The Office Action objects to claim 10 based on informalities. Claim 10 has been amended to obviate the objection by correcting claim dependency. Withdrawal of the claim objection is respectfully requested.

The Office Action rejects claims 5-7 under 35 U.S.C. §102(e) over U.S. Patent 6,252,266 to Hoshi *et al.* (Hoshi). This rejection is respectfully traversed.

Hoshi does not teach or suggest a method to manufacture a semiconductor device, comprising preparing a semiconductor wafer including a plurality of semiconductor chip forming sections each having an electrode forming a first through hole in the electrode, forming a second through hole penetrating the semiconductor wafer and coaxial to the first through hole, the second through hole communicating with the first through hole, and forming a conduction layer that extends via the first and second through holes from a first surface of each of the semiconductor chip forming sections on which the electrode is formed to a second surface opposite to the first surface, the conduction layer being electrically connected to the electrode, as recited in claim 5. These reasons apply by extension to claims 6 and 7 based on their dependence from claim 5.

For example, the specification discloses various exemplary aspects of a method to manufacture a semiconductor device from a semiconductor wafer (5) having several chip-

forming sections (3). Each section (3) has a passive surface (A) and an opposite active surface (B) and includes an electrode (2). A first through hole (50) is formed in the electrode (2), followed by a second through hole (58) formed in the wafer (5) and superposed over the first through hole (50) along the same longitudinal axis. First and second dielectric films (38, 40) cover the first and second through holes (50, 58), respectively. The through holes (50, 58) together form a complete through hole (4) from the passive surface (A) to the active surface (B) of the sections (3). A dielectric layer (10) may be formed over the first and second dielectric films (38, 40) along the overall through hole (4) and overlaid by a conduction layer (8) to electrically connect the surfaces of the electrode (2).

Instead, Hoshi discloses a field effect transistor (FET) 45 with a comb-shaped gate structure. In particular, Hoshi teaches a grounding electrode 47a formed on a substrate 48 that includes via holes 42a, 43a. The grounding electrode 47a is connected to an electrode 50 on the opposite side of the substrate 48 by the via holes 42a, 43a (col. 8, lines 37-57 and Figs. 11 and 12 of Hoshi). The via holes 42a, 43a in Hoshi are clearly not coaxial, as provided in Applicant's claimed features. Moreover, Hoshi fails to describe a semiconductor wafer with a plurality of electrode-equipped chip forming sections, as provided in the claims.

A claim must be literally disclosed for a proper rejection under §102. This requirement is satisfied "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference" (MPEP §2131). Applicant asserts that the Office Action fails to satisfy this requirement with Hoshi.

The Office Action further rejects claim 8 under 35 U.S.C. §103(a) over Hoshi in view of U.S. Patent 4,016,593 to Konishi *et al.* (Konishi); claims 9-11 under 35 U.S.C. §103(a) over Hoshi in view of U.S. Patent 6,720,641 to Birdsley *et al.* (Birdsley); claim 12 under 35 U.S.C. §103(a) over Hoshi in view of U.S. Patent 5,843,821 to Tseng; and claim 13 under 35 U.S.C. §103(a) over Hoshi in view of U.S. Patent 6,221,769 to Dhong *et al.* (Dhong) and

Silicon Processing for the VLSI Era, v. 1, 2/e by Wolf *et al.* (Wolf). These rejections are respectfully traversed.

Konishi, Birdsley, Tseng, Dhong and Wolf do not compensate for the deficiencies of Hoshi outlined above for claims 5-7. Nor does Konishi teach, disclose or suggest the additional features recited in claim 8; or Birdsley teach, disclose or suggest the additional features recited in claims 9-11; or Tseng teach, disclose or suggest the additional features recited in claim 12; or Dhong and Wolf teach, disclose or suggest the additional features recited in claim13.

Instead, Konishi discloses a bi-directional photothyristor. In particular, Konishi teaches a semiconductor substrate 51 having opposite surfaces 511, 512. The substrate 51 comprises layers N_1, P_1, N_3, P_2 and N_2, with P_1 and N_1 facing the first surface 511 and P_2 and N_2 sharing the second surface 512. Main electrodes 52, 53 are formed over the respective surfaces 511, 512, and a resin-filled through-hole 519 connects a light source 55 above the electrode 52 to a support plate 54 under the electrode 53 (col. 7, line 53 – col. 8, line37 and Figs. 5 and 6 of Konishi). The through-hole 519 exhibits a tandem-sloped groove or channel through the substrate 51, and hence has no relation to a first hole (through an electrode) being greater in size to a second through hole (through a wafer), as provided in Applicant's claimed features.

Further, Birdsley discloses a semiconductor structure 100. In particular, Birdsley teaches a substrate 102 and an electrically insulative layer 122. The substrate 102 forms body and well regions 104, 106 leading to electrical conductors 124, 126, 128, 130 that penetrate through the insulative layer 122. Birdsley further teaches a conductive probe 140 from a pad 144 on a surface of the substrate 102 opposite the insulative layer 122 and coupled to the body region 104 (col. 4, line 45 – col. 5, line 14 and Fig. 2 of Birdsley). There is no teaching

or suggestion of a dielectric film covering an electrode and coaxial through holes, as provided in Applicant's claimed features.

Also, Tseng discloses capacitor fabrication method. In particular, Tseng teaches forming a hole 44 by dry etching through an oxidation barrier layer 34 and into a conductive layer 30 (col. 6, lines 11-21 and Fig. 3 of Tseng). However, Tseng fails to teach or suggest dry etching a hole through an electrode, as provided in Applicant's claimed features.

Moreover, Dhong discloses connections through a wafer to an integrated circuit. In particular, Dhong teaches a silicon substrate 102 having vias 201. Dhong further teaches the substrate 102 and vias 201 being covered by a silicon nitride insulation barrier 203 (formed by CVD), and the vias filled with copper 205 (col. 6, lines 11-31 and Fig. 2 of Dhong). In addition, Wolf teaches electroplating using copper sulfate (section 15.8.3 of Wolf). However, neither Dhong nor Wolf teaches electroplating through holes, as provided in Applicant's claimed features.

Further, there is no motivation to combine features related to the multi-via FET of Hoshi with the grooved photothyristor of Konishi, the substrate-penetrating conductive probe of Birdsley, the conductive layer etching of Tseng, the copper-filled vias of Dhong, and/or the copper sulfate electroplating of Wolf, nor has the Office Action established sufficient motivation for a *prima facie* case of obviousness. Even assuming that motivation to combine the applied references is established, the combination fails to teach or suggest Applicant's claimed features.

A *prima facie* case of obviousness for a §103 rejection requires satisfaction of three basic criteria: there must be some suggestion or motivation either in the references or knowledge generally available to modify the references or combine reference teachings, a reasonable expectation of success, and the references must teach or suggest all the claim

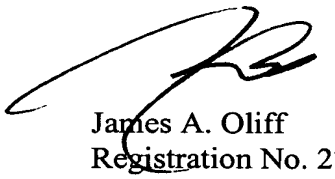
limitations (MPEP §706.02(j)). Applicant asserts that the Office Action fails to satisfy these requirements with Hoshi, Konishi, Birdsley, Tseng, Dhong and Wolf.

For at least these reasons, Applicant respectfully asserts that the independent claim is patentable over the applied reference. The dependent claims are likewise patentable over the applied references for at least the reasons discussed, as well as for the additional features they recite. Consequently, all pending claims are in condition for allowance. Thus, Applicant respectfully requests that the rejections under 35 U.S.C. §§102 and 103 be withdrawn.

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,



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